The IV fins **110** may be grown on the sidewalls of the mandrels **106** in the pFET and nFET regions **101**, **103** using any formation technique known in the art, such as, for example, epitaxial growth. Epitaxy growth may be a layer of monocrystalline semiconductor material which grows outward from an exposed surface of an existing monocrystalline semiconductor region or layer. The epitaxial layer may have the same composition as the semiconductor region on which it is grown, the same impurities (e.g., dopants and their concentrations), or, alternatively, the compositions of the epitaxial layer and the underlying semiconductor region can be different. The IV fins **110** may have a thickness ranging from about 2 nm to about 10 nm. Defects may begin to occur in epitaxial growth if a critical thickness is exceeded, the critical thickness may range from about 2 nm to about 10 nm. In an embodiment, the IV fins **110** may be selectively grown on the sidewalls of the mandrels **106** and not on the hardmask **108** or the buried insulator layer **104**, as illustrated. The IV fins **110** may be germanium and have a thickness of about 8 nm.

The IV fins **110** may be any material known in the art, such as, for example, germanium, silicon germanium, or other good pFET materials. In an embodiment, the IV fins **110** may be germanium. There may be a fin pitch between any two adjacent IV fins **110**. A first pitch (p**1**) may be between adjacent IV fins **110** in the pFET region **101** and a second pitch (p**2**) may be between adjacent IV fins **110** in the nFET region **103**. The first pitch (p**1**) may be the same as the second pitch (p**2**). In an embodiment, both the first pitch (p**1**) and the second pitch (p**2**) are equal to about 42 nm.

Referring now to FIG. **4**, a demonstrative illustration of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface is provided, according to an exemplary embodiment. More specifically, the method can include removing the hardmask **108** and the mandrels **106**.

The hardmask **108** and the mandrels **106** may be removed using any mask removal technique as is known in the art, such as, for example, RIE. The etching technique used to remove the mandrels **106** may etch the mandrels **106** selective to the IV fins **110** and the buried insulator layer **104** (i.e., etching the mandrels **106** and using the IV fins **110** and the buried insulator layer **104** as an etch stop). An alternative method may include depositing a protective material on the buried insulator layer **104** and etching the mandrels **106** selective to the IV fins **110**.

Referring now to FIG. **5**, a demonstrative illustration of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface is provided, according to an exemplary embodiment. More specifically, the method can include forming a spacer layer **112** on the IV fins **110**.

The spacer layer **112** may be conformally formed on the IV fins **110** using any deposition technique known in the art, such as, for example, chemical vapor deposition, plasma enhanced chemical vapor deposition, or atomic layer deposition. The spacer layer **112** may have a thickness ranging from about 2 nm to about 15 nm. The spacer layer **112** may be any spacer material known in the art, such as, for example, an oxide or a nitride.

Referring now to FIGS. **6** and **7**, demonstrative illustrations of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface are provided, according to an exemplary embodiment. More specifically, the method can include removing the spacer layer **112** from a top surface and a side surface of the IV fins **110** in the nFET region **103**.

First, a mask **113** may be formed on the IV fins **110** in the pFET region **101** using any deposition and patterning technique known in the art, such as, for example, photolithography. The mask **113** may be any masking material known in the art, such as, for example, oxide, nitride, or oxynitrides.

Next, a portion of the spacer layer **112** may be removed from the top surface and the side surface of the IV fins **110** in the nFET region **103** by exposing the top surface and the side surface to an angled removal process **150**. A protected surface of the IV fins **110** may be a side opposite the side surface of the IV fins **110** in the nFET region **103** exposed to the angled removal process **150**. The angled removal process **150** may be any angled removal process known in the art, such as, for example, an angled ion implantation (damaging the spacer layer **112** on the top surface and the side surface of the IV fins **110** in the nFET region **103** and not damaging the spacer layer **112** on the protected surface) and a wet etch (removing the damaged spacer layer **112**) or an angled etch (e.g., gas cluster ion beam). The angled removal process **150** may expose a portion of the IV fins **110** on the top surface and the side surface of the IV fins **110** in the nFET region **103** (i.e., remove a covering portion of the spacer layer **112** from above the IV fins **110** in the nFET region **103**). The spacer layer **112** may remain on the protected surface of the IV fins **110** in the nFET region **103**. The mask **113** may be removed using any mask removal technique as is known in the art.

In an embodiment, a possible ion implantation for performing damage to the spacer layer **112** is Xenon ions at 5 keV to a concentration of $3\times10^{14}/cm^2$ at an angle of 30°. More generally, it is preferred to use relatively massive ions both as a matter of delivering a suitable level of kinetic energy to target materials and damaging the targeted materials to cause the materials to etch more rapidly. The ion implantation angle chosen should also assure the implantation into the entire height of the spacer layer **112** and may need to be adjusted if the IV fins **110** are formed in particularly close proximity to each other. Depending on the thickness of the spacer layer **112**, the implant dose can range from $2\times10^{13}/cm^2$ to $2\times10^{15}/cm^2$, the implant energy can range from about 0.5 KeV to about 100 KeV and the implant angle can range from 15° to 75°. Once the spacer layer **112** is damaged, a removal step may be performed to remove the damaged spacer layer **112** using any technique known in the art, such as, for example, a wet etch containing a solution of hydrofluoric acid as the etchant.

Referring now to FIGS. **8** and **9**, demonstrative illustrations of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface are provided, according to an exemplary embodiment. More specifically, the method can include forming the III-V fins **114** on the exposed portion of the IV fins **110** in the nFET region **103**.

The III-V fins **114** may be formed on the exposed portions of the IV fins **110** using any technique known in the art, such as, for example, epitaxial growth. The epitaxial growth of the III-V fins **114** may use the IV fins **110** as a seed layer. The spacer layer **112** may protect against the growth of III-V fins **114** on the IV fins **110** in the pFET region **101** and the protected surface of the IV fins **110** in the nFET region **103**. The III-V fins **114** may directly contact the buried insulator layer **104**; the III-V fins **114** and the IV fins **110** may share a bottom surface coplanar with a top surface of the buried insulator layer **104**. If the III-V fins **114** form on the top surface of the IV fins **110**, the III-V fins **114** may be removed from the top surface of the IV fins **110** using any removal technique known in the art, such as, for example, reactive